Low Power, High Speed PLL Fabricated In UTSi® Process

G. C. Wu, D. Kelly, D. Staab, and P. Denny

Peregrine Semiconductor Corporation, San Diego, CA 92121, U. S. A.

Abstract **A CMOS phase locked loop (PLL) design achieves GHz performance, low phase noise, low spurious side-bands and extremely low power (1V, 1GHz, and < 1mA of current.) The design is fabricated in 0.5μm UTSi® SOI process which has been previously described [1].**

I. Introduction

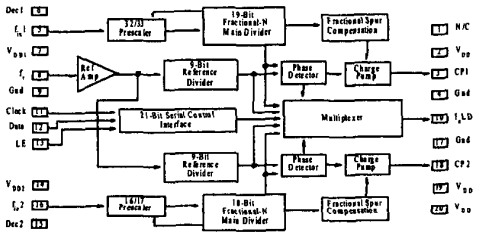
Today's mobile communication devices demand low power consumption in order to prolong precious battery life. For digital CMOS circuitry, power consumption can be expressed as Power $\propto CV^2f$, where V is the supply voltage, f is the frequency of operation and C is the nodal capacitance. Low power design requires a reduction of either C or V. Capacitance is generally limited by the process, so the supply voltage becomes the only degree of freedom. Voltage reduction is generally limited by the required speed of operation. Bulk CMOS devices are doubly penalized in this regard due to the body parasitics' dependence on applied voltage. These parasitic capacitances are inversely proportional to voltage. UTSi® CMOS has no bulk effect and consequently exhibits excellent switching speed at reduced supply voltages.

In this paper, a high speed and low power CMOS PLL manufactured using UTSi® CMOS is presented. This PLL utilizes a "FlexiPower," mode where power consumption is scaled for performance, on demand, simply by adjusting the voltage to the digital prescaler. This option gives the user the flexibility of using the device in various applications.

Also, novel techniques of phase detector and spurious side-band reduction circuit designs are described. All of these techniques contribute to a high performance PLL system.

II. Circuit Section

A. Top-level block diagram



B. 16/17 prescaler

The 16/17 prescaler is comprised of a high-speed front-end divide-by-4/5 section using dynamic CMOS D-flip flops (DFF) as shown in fig. 1. Dynamic circuits tend to exhibit poor low frequency performance because they contain storage nodes that leak charge when the operating frequency is too low. The divide-by-4 section that follows the 4/5 block is realized with static CMOS DFFs The static DFF feeds back a control signal to prevent storage node discharge. The static DFF block is necessitated for all the loop divider counters due to the progressively reduced frequency of operation as the signal propagates through the divider chain.

The dynamic DFF is made up of two transmission gate/inverter pairs as shown in fig. 2. The last inverter for QB is placed only where it is needed in order to reduce loading on the Q output. Low V_T devices were used in order to permit operation at low supply voltage. The V_T's are +0.3V for NMOS and -0.3V for PMOS. The inverter inputs are commonly referred to as the storage nodes of a dynamic DFF. The speed of the circuit is dependent on how fast these nodes can be charged and discharged. Performance data is illustrated in the "Measured Data" section.

The operating voltage for the 16/17 prescaler ranges from just under 1V to 3V. The FlexiPower feature mentioned in the introduction allows for prescaler operation at low voltages independent of the rest of the IC while, for example, a PLL charge pump operates at 3V to maintain signal to noise integrity for the VCO. This feature facilitates user selectable power dissipation in order to extend battery life. This allows for the prescaler to run no faster than a given application demands.

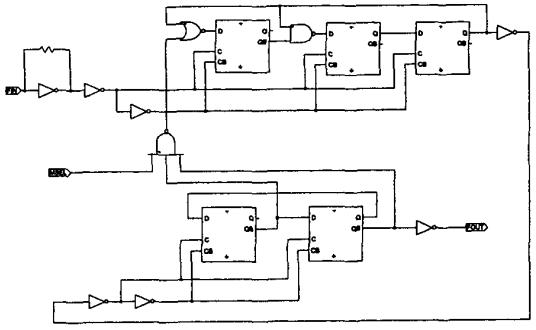


Fig. 1. 16/17 Dual Modulus Prescaler Schematic

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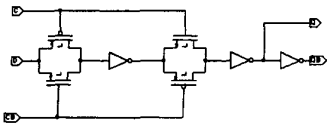

Fig. 2. DFF Schematic

UTSi® CMOS circuits operate at low supply voltages without severe degradation in the delay-power product. This benefit of UTSi® stems from several sources. The insulating sapphire substrate exhibits very low parasitic capacitance and requires no wells for device isolation. The simple equivalent circuit for a bulk silicon MOSFET is shown in fig. 3a. In this figure, the parasitic capacitances have been separated from the MOSFET, even though in practice they are an integral, inseparable part of the actual physical device. The circuit consists of a central "intrinsic" MOSFET, five capacitors, with four external connections called the gate, source, drain and bulk nodes. The capacitors Cgd and Cgs are similar in both bulk and UTSi®, and are physically caused by the overlapping of the source or drain with the gate and the charging and discharging of the inversion or channel region. The other three capacitances, Cgb, Cdb and Csb are very different between the bulk and UTSi® technologies. Cgb is the capacitance between the gate node and bulk node and is absent in a UTSi MOSFET. This capacitance has complex voltage dependence and is strongly dependent on geometry and process conditions [5].

Fig. 3b. illustrates the equivalent circuit for a UTSi®MOSFET. The source/drain nodes lay on sapphire instead of silicon. As with the bulk MOSFET equivalent circuit, the UTSi® circuit is comprised of a central "intrinsic" MOSFET. This MOSFET is connected to three capacitors and three external nodes called the gate, source and drain. The Cgd and Cgs capacitors are similar to their bulk counterparts and are physically caused by the overlap of the drain/source to gate regions plus the charging and discharging of the channel region. The sapphire substrate is a dielectric and, thus, the source/drain electric fields terminate on one another. This is represented by the parasitic capacitor, Csd. Csd is essentially voltage independent and is about one order or less in magnitude than the sum the values of Cdb and Csb in the bulk MOSFET. The transistor models used for circuit design do not contain the fourth terminal. Figure 4 illustrates the difference in nodal capacitance between bulk silicon and UTSi® devices.

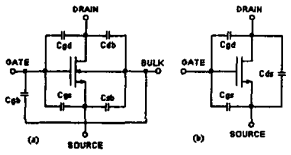

Fig. 3. (a) Bulk Si and (b) UTSi MOSFET.

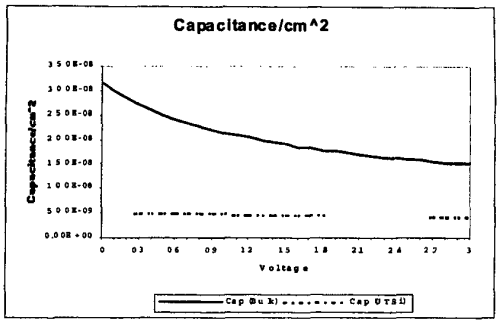

Fig. 4. Nodal capacitance vs. V_{DD} for bulk Si and UTSi CMOS.

Traditional high-speed designs typically employ bipolar ECL. These circuits are quite large as compared to digital CMOS. For reference, fig. 5 shows a side-by-side comparison of the digital CMOS prescaler (on the left) with its source-coupled logic (SCL) counterpart on the right. The SCL prescaler consumes approximately 4 times the die area of the identical circuit function realized in digital CMOS.

SCL:
X = 200 μm
Y = 310 μm

Digital CMOS
X = 110 μm
Y = 160 μm

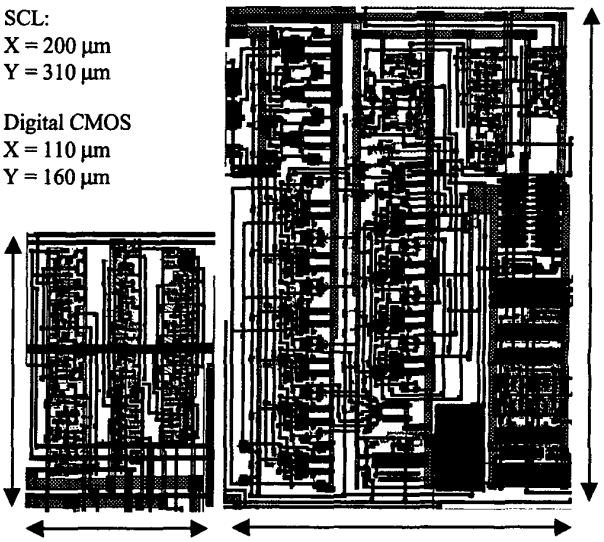

Fig. 5. Layout size comparison

C. Interface Level Shifting

Since the prescaler operates at 1V it is necessary to level shift its output to the divider stages that follow. An important advantage of UTSi® is the availability of multiple threshold transistors. 0V, 0.3V, and 0.7V are available for NMOS and 0V, -0.3V, and –0.7V are available for PMOS. The symbol for the low threshold (0.3V V_T) device is denoted schematically with the letter L, and similarly "i" is the intrinsic (0V V_T) and finally no label is the regular (0.7 V_T) device. The schematic in fig. 6 shows the interface circuit. The circuit operates as

follow. When the input is at 1V, N2 turns on and N1 turns off. Because N1 is "on" the output voltage drops and positive feedback turns P2 off. Even though N1 is a 0V V_T device, it will not draw current because a –1V V_{GS} voltage is applied. When the input is at 0V, N2 turns off and N1 turns on. Positive feedback in the PMOS cross-coupled pair turns P1 off and P2 on. When properly sized, the circuit is very fast. The only negative issue with this implementation is that N2 exhibits slight leakage currents when off.

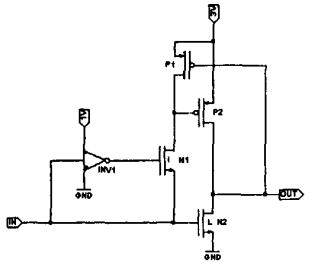

Fig. 6. 1V to 3V Translator Circuit

D. Charge Pump and Fractional-N Spurious Side-Band Reduction

The charge pump turn-on speed is designed to be fast to minimize reset delay in the phase detector for dead zone elimination. The charge pump uses the current steering principle. The tail current of the pull-up and pull-down is steered by a pair of differential cascode transistors to facilitate fastest response time. The tail current sources are made large to minimize their 1/f noise contribution. The differential cascode transistor pairs are made small to respond faster and to minimize switching charge injection into the output. The schematic is shown in fig. 7.

Also depicted in fig. 7 is the fractional-N spurious side-band reduction circuit. It is basically a capacitor and a switch [2]. In a fractional-N PLL, the phase detector comparison frequency is D times the channel step size, where D is the fractional denominator value. In an uncompensated fractional-N PLL using an accumulator, spurious side-bands occur at multiples of the channel step frequency. The presence of the switch, undersampling at exactly the channel step frequency, eliminates the spurious side-bands. In effect, the sampling places a zero at the spurious frequency and effectively notches out the resultant side-bands. With this extra sampling action, small charge pump leakage becomes less significant, however, it is critical that the sampling switch exhibit low leakage. Fortunately, in a locked loop, the operational V_{DS} for the switch transistors is near zero and the leakage is proportionally low.

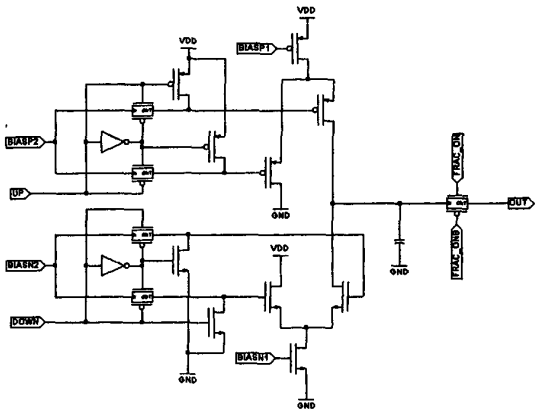

Fig. 7. Charge Pump and Fractional-N Spurious Side-band Reduction Circuit

E. Phase Detector

The conventional phase-frequency detector is shown in fig. 8. The inputs for the conventional phase detector typically come from the reference divider and main loop divider outputs. These outputs suffer significant accumulated edge jitter owing to the many stages that the signals must traverse. If these two signals are re-sampled by their respective clocks, one more DFF stage is necessary. In the proposed improved phase detector, the counter outputs are sampled at the same time the phase comparison takes place in the phase detector. As a result, the accumulated edge jitter in the digital counters is eliminated. The modified phase detector is represented in Fig. 9.

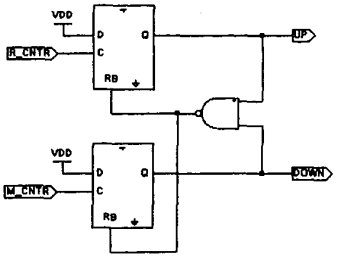

Fig. 8. Conventional Phase-Frequency Detector

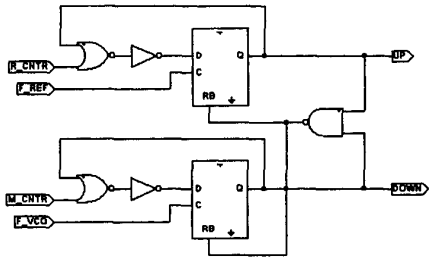

Fig. 9. Modified Phase Detector Schematic

F. Measured Results

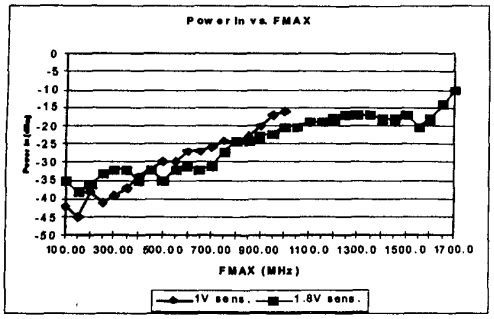

Fig. 10. P_{IN} versus F_{MAX} for V_{DD} = 1V and 1.8V (25C).

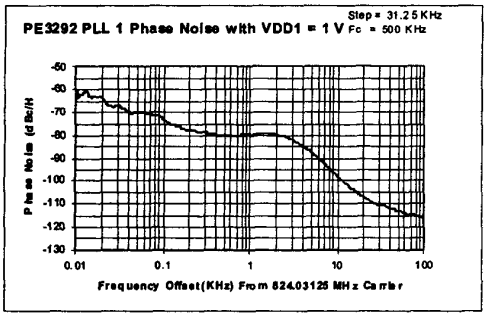

Fig. 11. Phase noise plot with FlexiV_{DD} = 1V (25C).

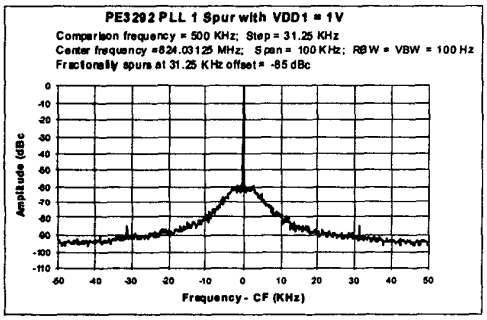

Fig. 12. Spurious sideband plot with FlexiV_{DD} = 1V (25C).

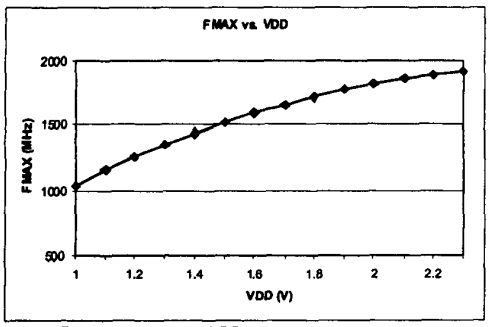

Fig. 13. Fmax vs. V_{DD} at 25C.

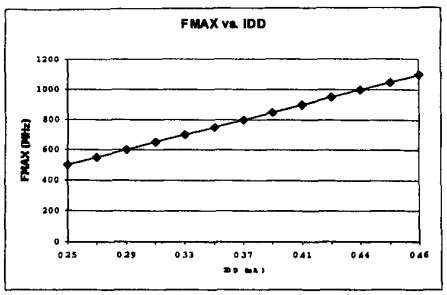

Fig. 14. Fmax vs. I_{DD} at 25C.

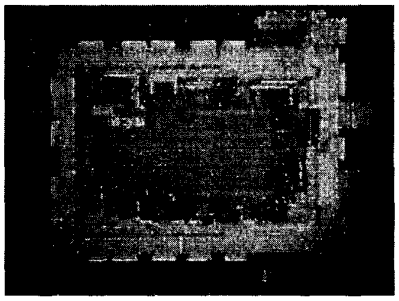

Fig. 15. Die Photo

III. Conclusion

In this paper, a low-power, high speed, low phase noise and low spurious side-band PLL is presented. The design captures and illustrates various benefits of UTSi® technology. As processing capability migrates toward 0.25µm, simulation shows speed improvement extending to 1.9 GHz F_{MAX} at 1 V V_{DD} and 1.5 mA. Furthermore, F_{MAX} performance at 1V is relatively insensitive to temperature variation according to simulation and measured results.

References

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[5] Wolf, Silicon Processing for the VLSI Era, Volume 3-The Submicron MOSFET, Chapter 5.